Remarks

Applicants have reviewed the Office Action mailed January 8, 2009. Claims 1–24 remain pending in the application and stand rejected. To better distinguish their invention from the art of record, applicants have amended claims 1, 9, 11, 19, and 20. No new matter has been added, and no amendment has been made which would require a new search.

Claims 1–24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over International Patent Publication WO 08/16040 to Adams (hereinafter "Adams") in view of U.S. Patent No. 5,956,674 to Smyth (hereinafter "Smyth") and in further view of European Patent Publication No. 0453063 to Fletcher (hereinafter "Fletcher").

Claim 1 as amended recites, *inter alia*, "wherein . . . the time separating a first set of successive identified transitions is a first measurement of said estimated bit time." Claims 11, 20, 23, and 24 recite analogous language. The Examiner asserts that Adams teaches this element in its discussion of shift register 53.

On page 8, Adams describes a technique for parsing the pulse lengths of a biphase data stream. Adams sets three taps to a signal at half-multiples of a time T defined as "the period of time for one cell in the biphase-mark encoded data input." (Adams, page 8, lines 11–12.) Adams adjusts the time T by adjusting the shift register's clock frequency. (Adams, page 9, lines 9–12.) Adams does this using a servo loop that performs continual adjustments, slowly increasing the frequency when processing data, and quickly dropping the frequency when a preamble is detected. (Adams, pages 9–11.) In particular, Adams describes how the circuit initially responds, giving examples of an initial frequency (and hence, an initial bit time) which is too high, and an initial frequency which is too low. (Adams, page 11, lines 1–13.) Adams does not describe any means for determining the initial frequency, or any means for determining an initial time T. Therefore, Adams relies on the prior art technique it described for selecting an initial frequency, a technique based upon the known frequency of the input signal. (Adams, page 5, lines 18–24.)

Therefore Adams does not disclose or suggest that a first measurement for an estimated bit time is the time separating a first set of successive identified transitions.

Fletcher fails to cure the deficiencies of Adams. Fletcher's estimation of bit times is unreliable initially. (Fletcher, col. 3, lines 30–52.) Fletcher teaches setting an initial value of zero for its average bit time. (Fletcher, col. 3, lines 32–34.) Doing so results in poor behavior initially so Fletcher has a fixed threshold comparator 20 which essentially sets a minimum bit time roughly equal to the shortest expected pulse. (Fletcher, col. 3, lines 47–50.) This threshold allows the Fletcher system to function while its average builds up from the initial value of zero, but ultimately decreases the flexibility as it sets a hard limit on the system's functional sampling rate, beyond which the threshold would improperly interpret all pulse lengths as "A" pulses.

Fletcher explicitly states that the first measurement for its average, and hence for its estimated bit time, is *zero*. Therefore, applicants respectfully assert that Fletcher fails to disclose or suggest a first measurement for an estimated bit time being the time separating a first set of successive identified transitions.

The Smyth patent fails to cure the deficiencies of Adams and Fletcher. Smyth is not directed at all to biphase encoding, and as such, the need to estimate a bit time does not arise. Applicants respectfully assert that Adams, Fletcher, and/or Smyth, taken alone or in any combination, fail to disclose or suggest a first measurement for an estimated bit time being the time separating a first set of successive identified transitions.

Furthermore, claim 23 recites, *inter alia*, "estimating minimum and maximum bit window times." Claim 9, 19, and 24 recite analogous language. The Examiner asserts that the Adams patent discloses this element in the form of the shift register shown in FIG. 11.

However, the basis for the Examiner's assertion remains unclear. Adam's shift register, serves to discriminate between different pulse lengths. Adams makes use of delay taps, with the delay length based on a continually adjusting servo loop, whereas the applicants' claimed invention constructs a timing window based on an estimated bit time. In order to estimate a bit time,

applicants estimate a bit window as described in the present application, pages 11 and 12. The bit window and timing window have ranges which represent different quantities. Adams does not have any analogue for bit window times.

As noted above, Adams determines a bit time T by a totally different mechanism and, as such, Adams does not disclose or suggests estimating minimum or maximum bit window times.

Fletcher fails to cure the deficiencies of Adams in this respect. Fletcher's technique for estimating bit times does not rely on bit windows, but instead builds a bit time estimate by progressively increasing the average value from an initial value of zero. Because Fletcher takes an alternate approach for estimating bit times, Fletcher has no need for bit window times. Therefore, applicants respectfully assert that Fletcher does not disclose or suggest estimating minimum or maximum bit window times.

As above, Smyth does nothing to cure the deficiencies of Adams and Fletcher. The Smyth patent does not concern itself with biphase encoding, and as such never deals with bit window times at all. Therefore, Adams, Fletcher, and/or Smyth, taken alone or in any combination, fail to disclose or suggest estimating minimum or maximum bit window times.

Claim 23 further recites, "constructing a bit window from said minimum and maximum bit window times." Claim 9, 19, and 24 recite analogous language. The Examiner asserts that these elements are disclosed by Adams in its summary.

The portion of Adams which the Examiner cites refers to "a coding scheme having a maximum pulse width." However, this section simply describes the general structure of biphase encoded data and says nothing regarding constructing a bit window, whether from minimum or maximum bit window times, or from any other value.

Furthermore, as noted above, Adams determines its time T by a totally different mechanism from the present invention and, as such, Adams never discloses or suggests estimating minimum or maximum bit window times. Adams also fails to disclose or suggest constructing a bit window from these minimum and maximum bit window times.

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Again, Fletcher fails to cure the deficiencies of Adams. Because Fletcher takes an alternate approach for estimating bit times, as noted above Fletcher has no need bit window times, and therefore it is respectfully asserted that Fletcher does not disclose or suggest constructing a bit window.

As above, Smyth does nothing to cure the deficiencies of Adams and Fletcher. Smyth is not concerned with biphase encoding, and as such never deals with bit windows at all. It is therefore respectfully asserted that Adams, Fletcher, and/or Smyth, taken alone or in any combination, fail to disclose or suggest constructing bit windows.

For at least the above reasons, it is respectfully asserted that Adams, Fletcher, and/or Smyth, taken alone or in any combination, fail to disclose or suggest all of the elements of claims 1, 11, 20, 23, and 24. It is therefore believed that claims 1, 11, 20, 23, and 24 are in condition for allowance. Furthermore, claims 2–10, 12–19, and 21–22 depend from claims 1, 11, and 20 respectively, and therefore include all of the elements of their parent claims. It is therefore believed that claims 2–10, 12–19, and 21–22 are also in condition for allowance. As noted above, claims 9 and 19 include patentable subject matter beyond that present in claims 1 and 11. It is therefore believed that claims 9 and 19 are separately patentable.

Conclusion

In view of the foregoing, applicants solicit entry of this amendment and allowance of the claims. If the Examiner cannot take such action, the Examiner should contact the applicant's attorney at (609) 734-6820 to arrange a mutually convenient date and time for a telephonic interview.

No fees are believed due with regard to this Amendment. Please charge any fee or credit any overpayment to Deposit Account No. **07-0832**.

Respectfully submitted,

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